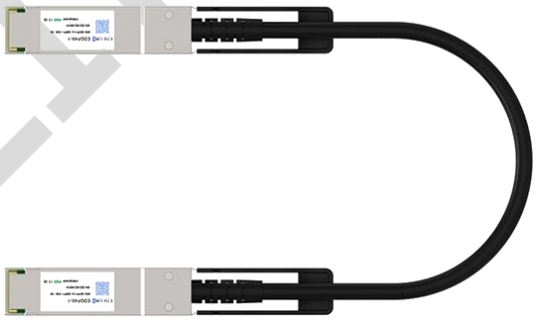
EDQP4X-x

40G QSFP+ Direct Attach Passive Copper Cables

PRODUCT FEATURES

- Maximum aggregate data rate: 40 Gb/s (4 x 10Gb/s)
- Support for multi-gigabit data rates :1 Gb/s - 10 Gb/s (per channel)
- QSFP+ conforms to the Small Form Factor SFF-8436
- 4-Channel Full-Duplex Passive Copper Cable
- Copper link length up to 5m (passive limiting)
- High-Density QSFP 38-PIN Connector
- Compatible to IEEE 802.3ba and SFF-8436
- Compatible to QSFP+ MSA
- Power Supply :+3.3V
- Low power consumption: 0.02 W (typ.)
- I2C based two-wire serial interface for EEPROM
- signature which can be customized
- Temperature Range: 0~ 70 °C
- Comply with RoHS 6.0



APPLICATIONS

- **10G/40G Ethernet**
- **InfiniBand 4x SDR/DDR/QDR**
- **2/4/8/10G Fibre Channel**
- **Fibre Channel over Ethernet**
- **SAS, Servers, Hubs, Switches, and Routers**

DESCRIPTIONS

40G QSFP+ direct attach passive cable uses shielded high-speed differential cable, whichIt conforms to 40g Ethernet ieee802.3ba standard and sff-8436 Qsfp+ standard, supports 40g transmission rate, and is also downward compatible with low rate applications. Qsfp+ passive cable is the preferred solution for 40g rate short distance application, which is widely used in data transmission between data center and cabinet or between adjacent cabinets. Its biggest characteristics are low cost, ultra-low power consumption (less than 0.1W) and high reliability.

Ordering Information

Part No.	Description
EDQP4X-x-30	40G QSFP+ Direct Attach Passive Copper Cables (DAC) 0~3M 30AWG
EDQP4X-x-26	40G QSFP+ Direct Attach Passive Copper Cables (DAC) 3~5M 26AWG
EDQP4X-x-24	40G QSFP+ Direct Attach Passive Copper Cables (DAC) 7M 24AWG

Notes:

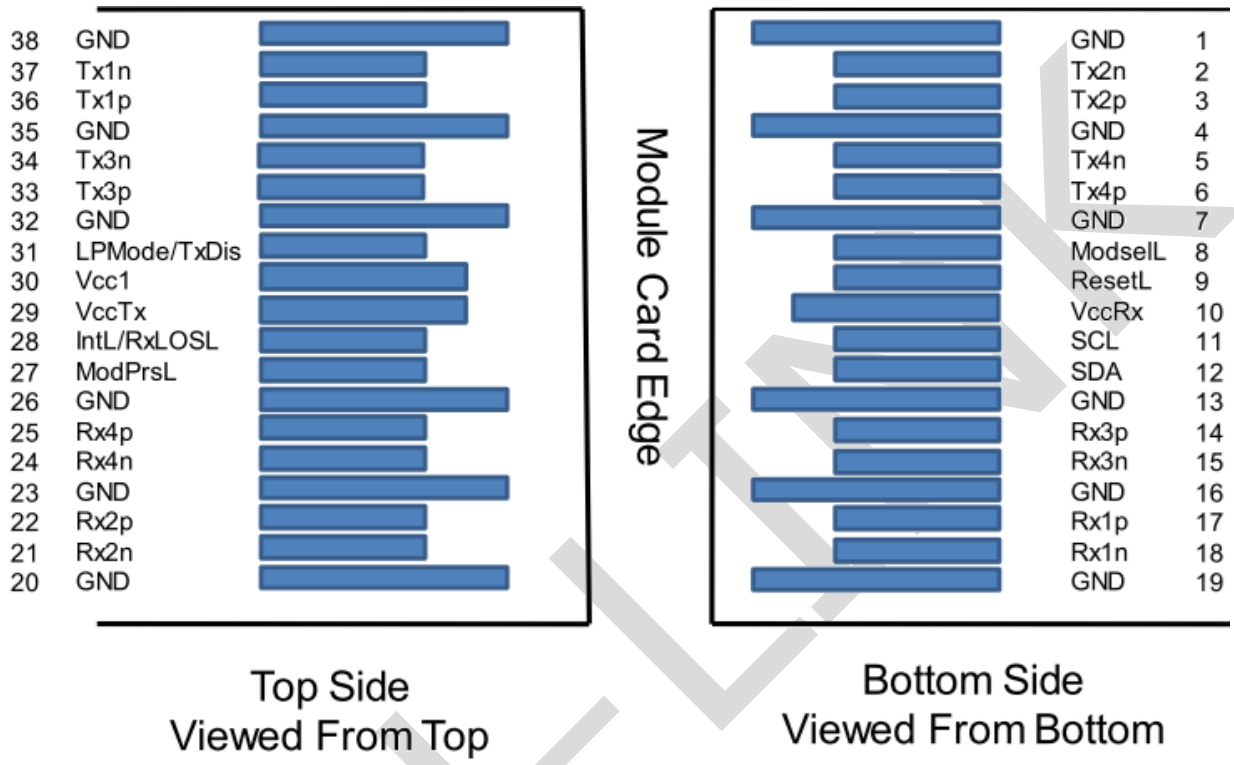
1. where "x" denotes cable length in meters. Examples are as follows:
2. x = 1 for 1m,

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Storage Ambient Temperature		-40		85	°C
Operating Case Temperature	Tc	0		+70	°C
Power Supply Voltage	VCC3	3.14	3.3	3.47	V

Power consumption	PD			0.2	W
Data Rate Per Lane		1		41.2	Gb/s

QSFP+ DAC-end Pin Diagram



Pin Descriptions

PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	

10		Vcc Rx	+ 3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CMLO	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CMLO	Rx1p	Receiver Non-Inverted Data Output	
18	CMLO	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CMLO	Rx2n	Receiver Inverted Data Output	
22	CMLO	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CMLO	Rx4n	Receiver Inverted Data Output	1
25	CMLO	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTLO	ModPrsL	Module Present	
28	LVTTLO	IntL	Interrupt	
29		Vcc Tx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTLI	LPMode	Low Power Mode	
32		GND	Ground	1
33	CMLI	Tx3p	Transmitter Non-Inverted Data Input	
34	CMLI	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CMLI	Tx1p	Transmitter Non-Inverted Data Input	
37	CMLI	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

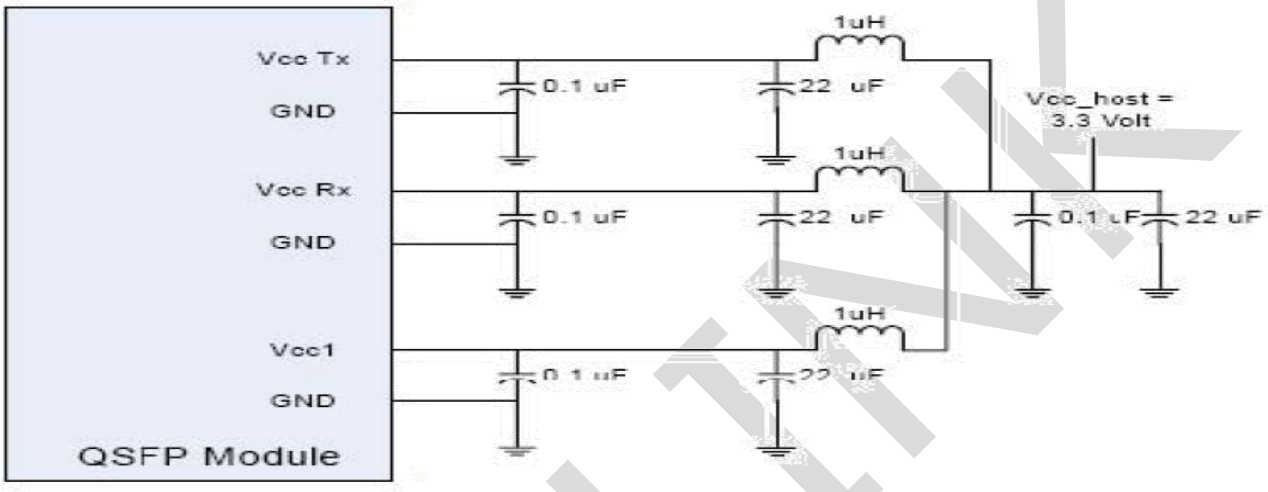
Notes:

1) GND is the symbol for signal and supply (power) common for QSFP modules. All are common within the QSFP module and

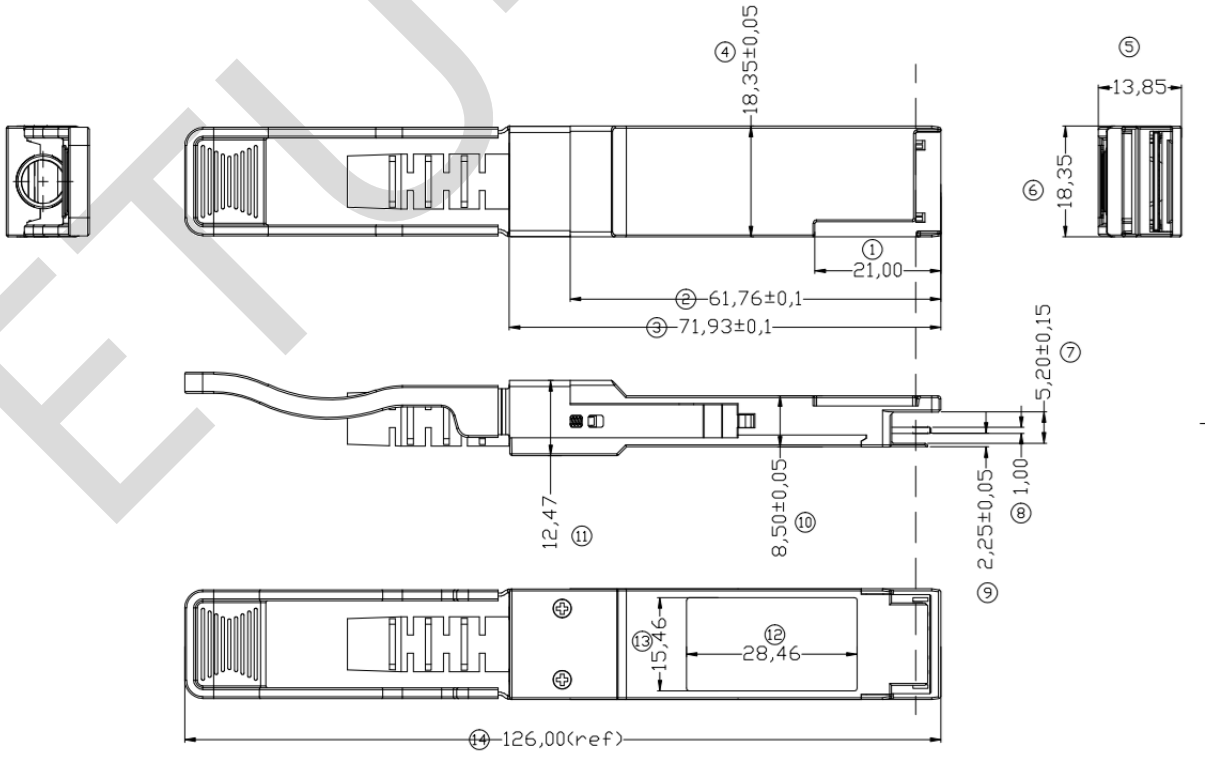
all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane.

2) Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

Power Supply Filtering



Mechanical Diagram



Revision History

Version No.	Date	Description
1.0	February 8, 2019	Preliminary datasheet
2.0	Aug 12,2024	Format change

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