EB894X-01D-R

40Gbps QSFP+ BIDI Receiver module, Multi Mode, 100m Reach

PRODUCT FEATURES

- **Compliant to the 40GbE XLPPI electrical specification per IEEE 802.3ba-2010**
- **Compliant to QSFP+ SFF-8436 Specification**
- **Aggregate bandwidth of > 40Gbps**
- **Duplex LC connector Only Receiver**
- **Operates at 10.3125 Gbps per electrical channel with 64b/66b encoded data**
- **QSFP MSA compliant**
- **Integrated ROSA for up to 100m reach over OM3 Multimode Fiber (MMF)and reach over 150m on OM4 MMF**
- **Single +3.3V power supply operating**
- **Without digital diagnostic functions**
- **Temperature range 0°C to 70°C**
- **RoHS Compliant Part**
- **Utilizes a standard LC duplex fiber cable allowing reuse of existing cable infrastructure**

APPLICATIONS

- **40 Gigabit Ethernet interconnects**
- **Datacom/Telecom switch & router connections**
- **Data aggregation and backplane applications**
- **Proprietary protocol and density applications**

DESCRIPTIONS

The ETU-Link's EB894X-01D-R receiver integrates receiver on one module. It is a two-Channel,Pluggable, LC Duplex, Fiber-Optic QSFP+ Transceiver for 40 Gigabit Ethernet Applications. This transceiver is a high performance module for short-range duplex data communication and interconnect applications. It integrates four electrical data lanes in each direction into transmission over a single LC duplex fiber optic cable. Each electrical lane operates at 10.3125 Gbps and conforms to the 40GE XLPPI interface.

The transceiver internally multiplexes an XLPPI 4x10G interface into two 20Gb/s electrical channels, receiving each optically over one simplex LC fiber using bi-directional optics. This results in an aggregate bandwidth of 40Gbps into a duplex LC cable. This allows reuse of the installed LC duplex cabling infrastructure for 40GbE application. Link distances up to 100 m using OM3 and 150m using OM4 optical fiber are supported. These modules are de- signed to operate over multimode fiber systems using a nominal wavelength of 850nm on one end and 900nm on the other end. The electrical interface uses a 38 contact QSFP+ type edge connector. The optical interface uses a conventional LC duplex connector.

Ordering Information

Part No.	Data Rate(optical)	Fiber Type	Distance	Optical Interface	Temp	DDMI
EB894X-01D-R	40Gbps	MMF	100M	LC	0~70℃	Y

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T_S	-40	+85	℃	
Supply Voltage	V_{CC}	-0.5	4	V	
Relative Humidity	RH	0	85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Notes
Case Temperature- Operating	T_{CASE}	0	70	℃	
Supply Voltage	V_{CC}	+3.13	3.47	V	

Power Consumption	I_{CC}		1000	mA	
Power Consumption- LP Mode	$P_{DISS-LP}$		3.5	W	

Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Data Rate per Channel			10.3125		Gb/s	
Power Consumption		-	2.5	3.5	W	
Supply Current	I_{CC}		0.75	1.0	A	
Control I/O Voltage-High	VIH	2.0		Vcc	V	
Control I/O Voltage-Low	VIL	0		0.7	V	
Inter-Channel Skew	TSK			150	Ps	
RESETL Duration			10		Us	
RESETL De-assert time				100	ms	
Power On Time				100	ms	1
Receiver						
Single Ended Output Voltage Tolerance		0.3		4	V	
Rx Output Diff Voltage	Vo		600	800	mV	
Rx Output Rise and Fall Voltage	Tr/Tf			35	Ps	1
Total Jitter	TJ			0.7	UI	
Deterministic Jitter	DJ			0.42	UI	

Notes:

1. 20%~80%

Optical and Characteristics

Receiver Parameter	Lane	Min	Typical	Max	Unit	Notes
Optical Wavelength CH1	λ	882	900	868	nm	
Optical Wavelength CH2	λ	832	850	868	nm	
Receiver Sensitivity per Channel	R		-11		dBm	
Maximum Input Power	PMAX	+0.5			dBm	
Receiver Reflectance	Rrx			-12	dB	

LOS De-Assert	LOSD			-14	dBm	
LOS Assert	LOSA	-30			dBm	
LOS Hysteresis	LOSH	0.5			dB	

Notes:

1. 12dB Reflection

Timing for Soft Control and Status Functions

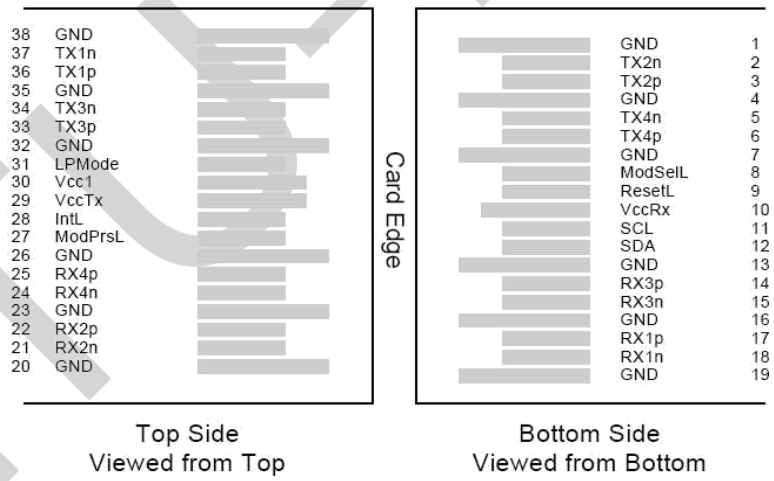
Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on1, hot plug or rising edge of Reset until the module is fully functional2
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on1 until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on1 to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional2
LPMode Assert Time	ton_LPMode	100	μs	Time from assertion of LPMode (Vin:LPMode =Vih) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	μs	toff_IntL 500 μs Time from clear on read3 operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set4 until associated IntL assertion is inhibited

Mask De-assert Time	toff_mask	100	ms	Time from mask bit cleared4 until associated IntlL operation resumes
ModSelL Assert Time	ton_ModSelL	100	μs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelL Deassert Time	toff_ModSelL	100	μs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set 4 until module power consumption enters lower
Power_over-ride or Power-set De-assert Time	toff_Pdown	300	ms	Time from P_Down bit set 4 until module power consumption enters lower

Note:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 de-asserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

Pin Diagram



Pin Definitions

PIN	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1

2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	

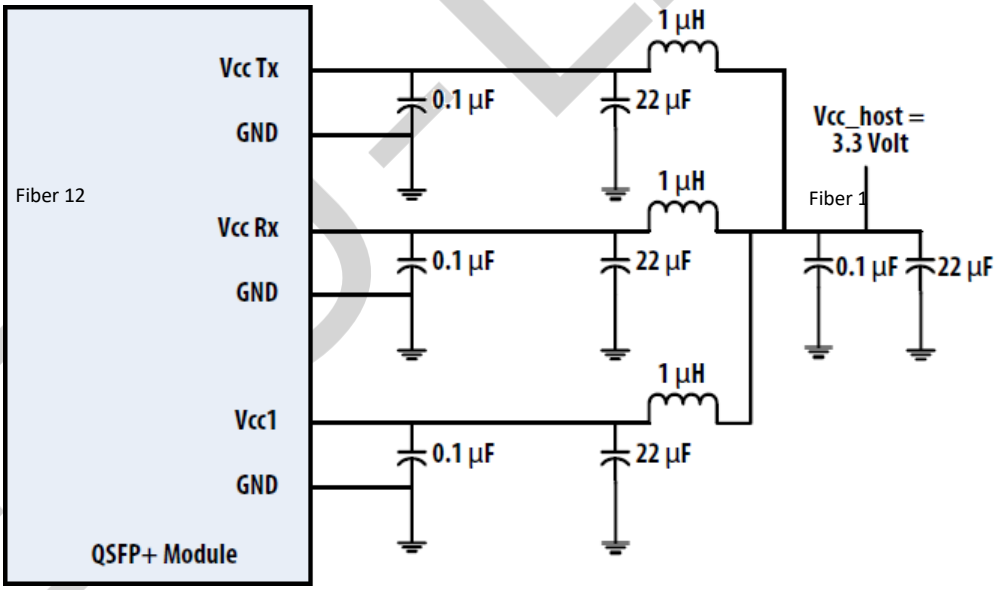
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Notes:

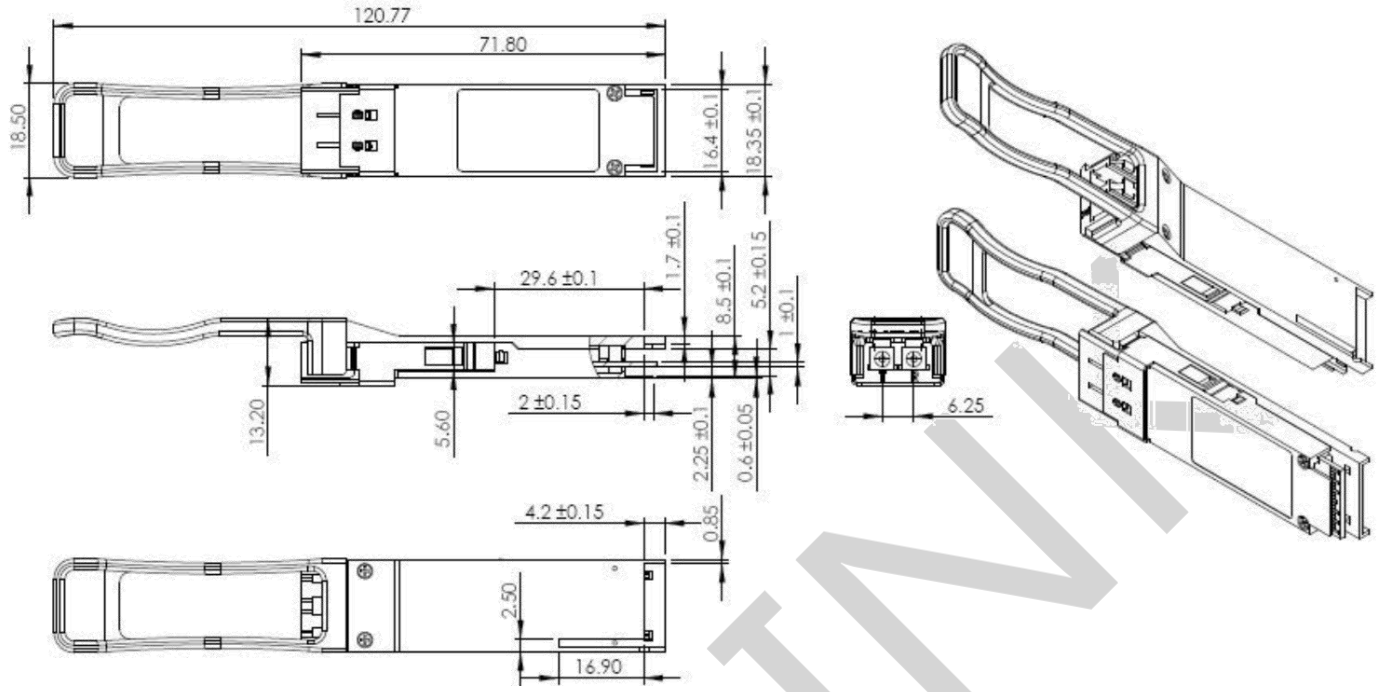
1. GND is the symbol for single and supply(power) common for QSFP modules, All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane. Laser output disabled on TDIS >2.0V or open, enabled on TDIS <0.8V.

2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for maximum current of 500mA.

Recommended Power Supply Filter



Mechanical Diagram



Revision History

Version No.	Date	Description
1.0	February 18, 2021	Preliminary datasheet
2.0	Aug 20,2024	Format change

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