

EDQP4X-4SPx

40G QSFP+ to 4 SFP+ Direct Attach Passive Copper Cables

PRODUCT FEATURES

- > Connector A: (1) QSFP 40.0 Gbps Rated Connector (SFF-8436 Compliant)
- > Connector B: (4) SFP+ 10.0 Gbps Rated Connectors (SFF-8431 Compliant)
- > Economically Links up a QSFP port with an Upstream 10GbE-SFP+ Switch
- > Protocol agnostic support of 40GbE, QDR InfiniBand, SAS & Fibre Channel
- > Up to 10.3125 Gbps transfer rate per SFP+ channel (40 Gbps aggregate)
- > Robust Zinc die-cast SFP+ & QSFP connectors with pull-to-release latching
- > Bridge the gap between your 10G and 40G capable switches/host adapters
- > Low cross-talk and pair-to-pair skew maintains signal integrity
- > Fully compliant to the latest SFP+ & QSFP MSA (Multi-Source-Agreement)
- > Supports all current 10-Gigabit Ethernet and 40-Gigabit Ethernet standards
- > Designated form factor and electrical compliance for QDR InfiniBand
- > The perfect direct attached storage splitter cable for Fibre Channel & SAS
- > Enjoy a reduced power budget and lower port cost compared to optical
- > Fully RoHS compliant for environmental protection

APPLICATIONS



- > 10G/40G Ethernet
- > InfiniBand 4x SDR/DDR/QDR
- > 2/4/8/10G Fibre Channel
- > Fibre Channel over Ethernet
- > SAS, Servers, Hubs, Switches, and Routers

DESCRIPTIONS

40G QSFP+ to 4x 10G SFP+ direct attach passive copper cable are suitable for very short distances and offer a highly cost-effective way to establish a 40-Gigabit link between QSFP+ and SFP+ equipment connections. These cables are used for 40GbE and Infniband standards, to maximize performance. QSFP+ are designed to meet emerging data center and high performance computing application needs for a high density cabling interconnect system capable of delivering an aggregate data bandwidth of 40Gb/s. This interconnect system is fully compliant with existing industry standard specifications such as the QSFP MSA and IBTA (InfiniBand Trade Association). The QSFP+ cables support the bandwidth transmission requirements as defined by IEEE 802.3ba (40 Gb/s) and Infiniband QDR (4x10 Gb/s per channel) specifications.

Ordering Information

Part Number	Product Description
EDQP4X-4SPx-30	40G QSFP+ to 4SFP+ Direct Attach Passive Cable, 1~3m, AWG:30 , 0°C ~ +70°C
EDQP4X-4SPx-24	40G QSFP+ to 4SFP+ Direct Attach Passive Cable, $3\sim5m$, AWG:24 , $0^{\circ}C \sim +70^{\circ}C$

Notes:

- 1. where "x" denotes cable length in meters. Examples are as follows:
- 2. x = 1 for 1m,

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-40	125	degC	
Relative Humidity (non-condensation)	RS	-	85	%	

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Operating Case Temperature	Торс	-5	75	degC	1
Supply Voltage	VCC3	-0.3	3.6	V	
Voltage on LVTTL Input	Vi _{lvttl}	-0.3	VCC3 +0.2	V	

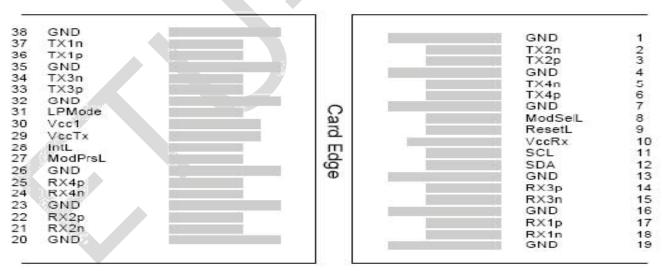
NOTE

Stress or condition sexceed the above range may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not applied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Торс	-5	75	degC
Relative Humidity (non-condensation)	RS		85	%
Supply Voltage	VCC3	3.135	3.465	V
Power Supply Current	ICC3	750	-	mA
Total Power Consumption	Pd	-	2.0	W

Pin Diagram



Top Side Viewed from Top Bottom Side Viewed from Bottom



Pin Definitions

PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		Vcc Rx	+ 3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CMLO	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CMLO	Rx1p	Receiver Non-Inverted Data Output	
18	CMLO	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CMLO	Rx2n	Receiver Inverted Data Output	
22	CMLO	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CMLO	Rx4n	Receiver Inverted Data Output	1
25	CMLO	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTLO	ModPrsL	Module Present	
28	LVTTLO	IntL	Interrupt	
29		Vcc Tx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTLI	LPMode	Low Power Mode	
32		GND	Ground	1
33	CMLI	Tx3p	Transmitter Non-Inverted Data Input	
34	CMLI	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CMLI	Tx1p	Transmitter Non-Inverted Data Input	
37	CMLI	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

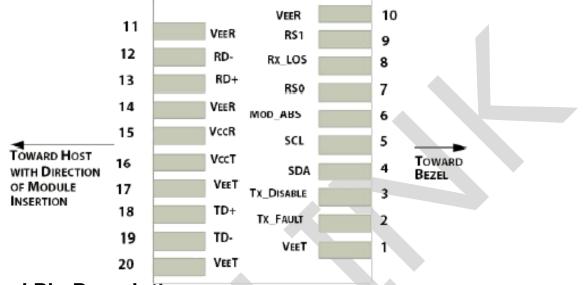
1. GND is the symbol for signal and supply (power) common for QSFP modules. All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane.



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2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

SFP+ end Pin Diagram



SFP+ end Pin Descriptions

PIN	Symbol	Name/Description	Note
1	VeeT	Transmitter Signal Ground	Note 1
2	TX_FAULT	Transmitter Fault (LVTTL-O) – Not used. Grounded inside the module	Note 2
3	TX_DISABLE	Transmitter Disable (LVTTL-I) – High or open disables the transmitter	Note 3
4	SDA	Two Wire Serial Interface Data Line (LVCMOS – I/O)	Note 4
		(same as MOD-DEF2 in INF-8074)	
5	SCL	Two Wire Serial Interface Clock Line (LVCMOS – I/O)	Note 4
		(same as MOD-DEF1 in INF-8074)	
6	MOD_ABS	Module Absent (Output), connected to VeeT or VeeR in the module	Note 5
7	RS0	Rate Select 0 - Not used, Presents high input impedance.	
8	RX_LOS	Receiver Loss of Signal (LVTTL-O)	Note 2
9	RS1	Rate Select 1 - Not used, Presents high input impedance.	
10	VeeR	Receiver Signal Ground	Note 1
11	VeeR	Receiver Signal Ground	Note 1
12	RD-	Receiver Data Out Inverted (CML-O)	
13	RD+	Receiver Data Out (CML-O)	
14	VeeR	Receiver Signal Ground	
15	VccR	Receiver Power + 3.3 V	
16	VccT	Transmitter Power + 3.3 V	
17	VeeT	Transmitter Signal Ground	Note 1

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18	TD+	Transmitter Data In (CML-I)	
19	TD-	Transmitter Data In Inverted (CML-I)	
20	VeeT	Transmitter Signal Ground	Note 1

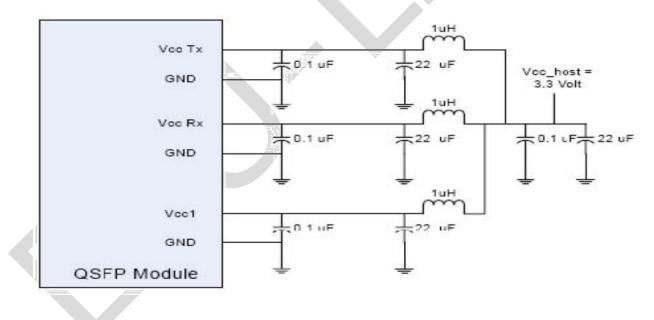
Notes:

- 1) Module circuit ground is isolated from module chassis ground within the module. GND is the symbol for signal and supply (power) common for SFP modules.
- This is an open collector/drain output that on the host board requires a 4.7 kΩ to 10 kΩ pullup resistor to VccHost. See Figure 2.
- 3) This input is internally biased high with a 4.7 k Ω to 10 k Ω pullup resistor to VccT.
- 4) Two-Wire Serial interface clock and data lines require an external pullup resistor dependent on the capacitance load.
- 5) This is a ground return that on the host board requires a 4.7 k Ω to 10 k Ω pullup resistor to VccHost.

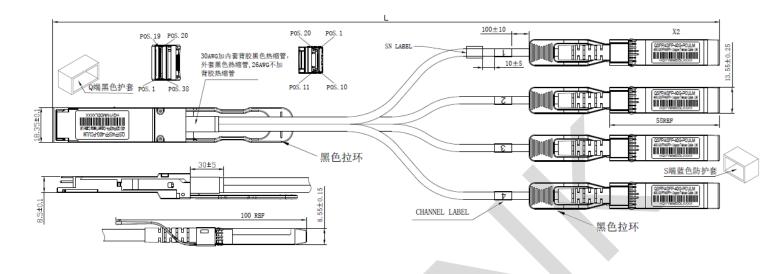
Recommended power supply filtering Example of QSFP Host

board schematics.

A typical host board mechanical layout for attaching the QSFP transceiver is presented below. The recommended host electrical connector should be a 38-pin IPASS right angle connector assembly and the cage assembly should be QSFP single cage.



Mechanical Dimensions



Revision History

Version No.	Date	Description
1.0	February 8, 2018	Preliminary datasheet
2.0	Aug 16,2024	Product upgrades

Company: ETU-Link Technology Co., LTD

Production base: Right side of 3rd floor, No. 102 building, Longguan expressway, Dalang street,

Longhua District, Shenzhen city, GuangDongProvince, China 518109

R&D base: Floor 4, Building 4, Nanshan Yungu Phase Ll, Taoyuan Community, XiliStreet,Nanshan District, Shenzhen

Tel: +86-755 2328 4603

Addresses and phone number also have been listed at www.etulinktechnology.com. Please e-mail us at sales@etulinktechnology.com or call us for assistance.