EAQD400-xxx

400G QSFP-DD Active Optical Cable

PRODUCT FEATURES

- **Up to 53. 125Gbps Data Rate per Channel by PAM4 Modulation**
- **Support 400GAUI-8 Electrical Interface**
- **Integrated 850nm VCSEL Array and PD Array**
- **DDM Function Implemented**
- **Hot-pluggable QSFP-DD Form Factor**
- **Maximum Link Length of 100m OM4 (MMF) Fiber**
- **Low Power Dissipation : ≤11W**
- **Single +3.3V Power Supply**
- **Operating Temperature Range : 0□~+70 □**
- **Compliant with RoHS**

APPLICATIONS

- **Data centers and Cloud**
- **Networks**

STANDARDS

- **IEEE 802.3cd**
- **QSFP-DD MSA**
- **CMIS4.0**

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DESCRIPTIONS

The 400G AOC is a QSFP-DD to QSFP-DD active optical cable for short-range data communication and interconnect applications. Each AOC has 8 duplex channels with 425Gbit/s aggregate bandwidth. Each channel operates with PAM4 modulation scheme at 53.125G baud rate, and up to 60m using OM3 fiber or 100m using OM4 fiber.

Ordering Information

Part No.	
EAQD400-xxx-OM3	400G QSFP-DD to QSFPDD Active Optical Cable OM3 0.5~100M

Note:

1. where "x" denotes cable length in meters. Examples are as follows:
x = 1 for 1m, xx=10 for 10m

Product	Electrical mode	Protocol	Nominal Rate			Specifications		Link
			Aggregate (Gbps)	Electrical Lanes(Gbaud)	ppm	High Speed Electrical	Pre-FEC Max BER	
EAQD400-xxx-OM3	8X50	IEEE802.3cd	425	26.5625 PAM4	±100	400GAUI-8	2.4E-4	0.5~100m

Absolute Maximum Ratings

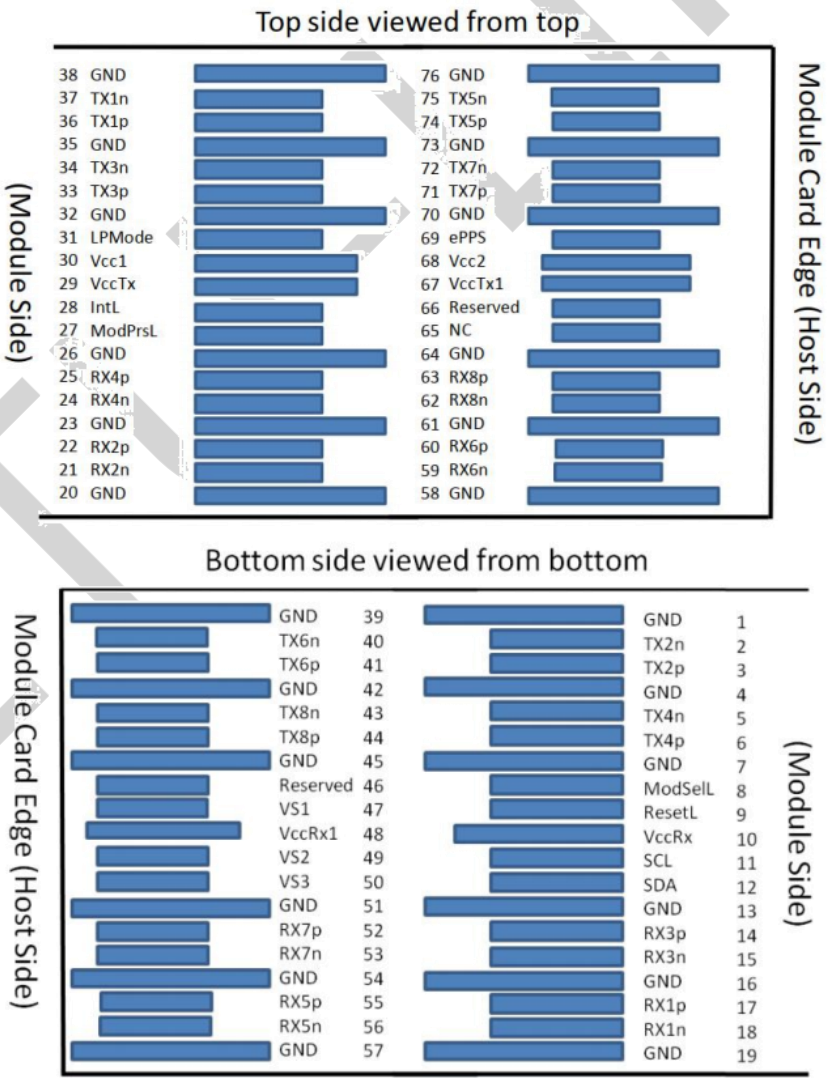
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	T_{STG}	-5	-	+75	ºC	
Relative Humidity (non-condensation)	R_H	5	-	85	%	
Power Supply Voltage	V_{CC}	-0.5	-	+3.6	V	

Electrical Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Supply Voltage	VCC	V	3.135	3.3	3.465	
Power Consumption	Pc	W			8	per end
Transmitter						
Input Differential Impedance	R_{IN}	Ω	80	100	120	
Single Ended Data Input Swing	V_{IN}	mVp-p	90		500	
Transmit Disable Voltage	V_{DIS}	V	2		V_{CCHOST}	

Transmit Enable Voltage	V_{EN}	V	VEE		V_{EE}+0.8	
Transmit Fault Assert Voltage	V_{FA}	V	2		V_{CCHOST}	
Transmit Fault De-Assert Voltage	V_{FDA}	V	VEE		V_{EE}+0.8	
Receiver						
Single Ended Data Output Swing	V_{OD}	mVp-p	200		500	
LOS Fault	V_{LOSFT}	V	2		V_{CCHOST}	
LOS Normal	V_{LOSNR}	V	VEE		V_{EE}+0.8	
Differential termination mismatch		%			10	
IIC communication						
IIC Clock frequency	-	KHZ	/	100	400	
clock stretching	-	us	/	/	500	

Pin Diagram



Pin Definitions

Pin	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16	GND	GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	1
18	CML-O	Rx1n	Receiver Inverted Data Output	1
19		GND	Ground	
20		GND	Ground	
21	CML-O	Rx2n	Receiver Inverted Data Output	1
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	
27	LVTTL-O	Mod PrsL	Module Present	2
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636)	2
29		VccTx	+3.3V Power supply transmitter	
30		Vcc1	+3.3V Power supply	1

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31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32		GND	Ground	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	1
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	1
37	CML-I	Tx1n	Transmitter Inverted Data Input	1
38		GND	Ground	
39		GND	Ground	
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	

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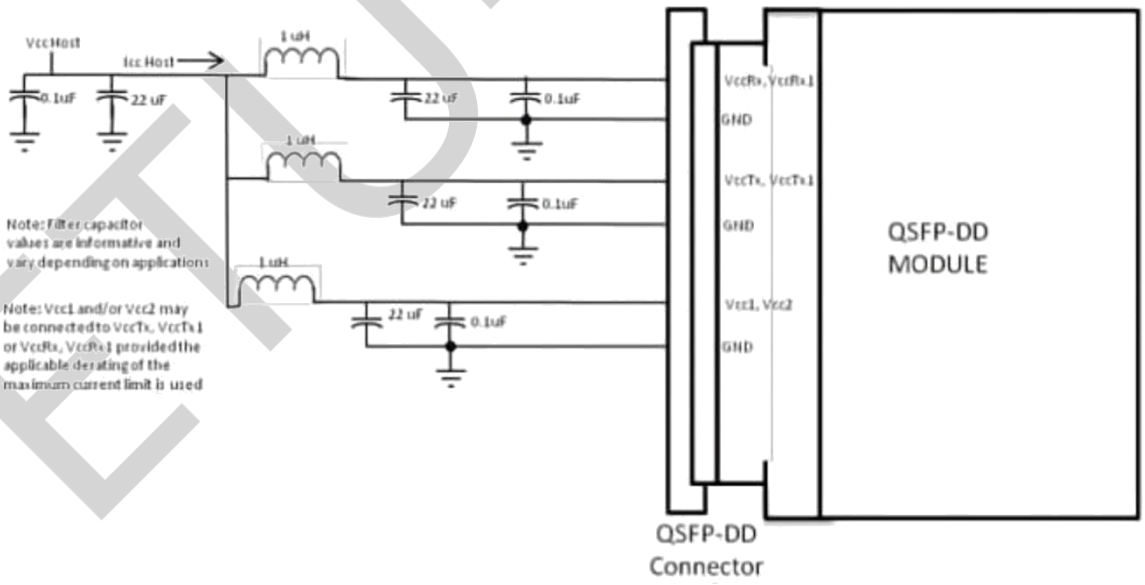
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future Use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		Reserved	For future Use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

Recommended Interface Circuit



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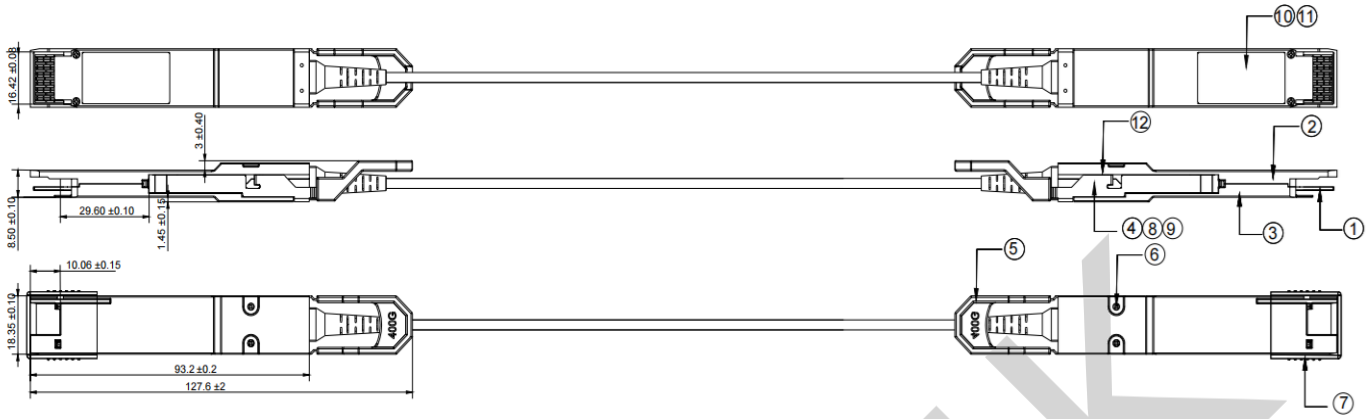
Mechanical Diagram



Parameter	Value	Units
Diameter	3±0 .2	mm
Minimum bend radius	30	mm
Length tolerance	1 m ≤length ≤ 4.5 m +15 / -0	cm
	5 m ≤length ≤ 14 .5 m +30 / -0	cm
	Length≥15 .0 m +2% / -0	m
Cable color	Aqua	

Revision History

Version No.	Date	Description
1.0	September 28,2022	Product upgrades

Company: ETU-Link Technology Co., LTD
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