EQD400-SR4

400G QSFP-DD SR4 Optical Transceiver

PRODUCT FEATURES

- Up to 106.25 Gbps data rate per channel by PAM4 modulation
- Integrated 850nm VCSEL array and PD array
- MPO-12 Receptacle
- Up to 100m transmission with OM4 MMF
- DDM function implemented
- Hot-pluggable
- Single +3.3V power supply
- Compliant to QSFP-DD HW Rev 6.2
- Compliant with CMIS 5.1
- 4x106. 25Gb/s electrical interface(400GAUI-4)
- Maximum power consumption 8W
- Single +3.3V power supply
- Case temperature range: 0 ~ +70C
- RoHS 2.0 complaint

APPLICATIONS

- 400G Ethernet
- Data Center Interconnect
- Enterprise Networking

Description

This product is a 400Gb/s QSFP-DD 400G SR4 optical module designed for 100m optical communication applications. The module converts 4 channels of 100Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 400Gb/s.

On the receiver side, the module converts 4 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 400Gb/s into 4channels of 100Gb/s (PAM4) electrical output data.

An optical fiber cable with a single MPO-12 connector can be plugged into the QSFP-DD 400G SR4 module receptacle. Host FEC is required to support up to 100m fiber transmission.

Ordering information

Part No.	Data Rate	Laser	Fiber Type	Distance	Optical Interface	Temp	DDMI
EQD400-SR4	400Gbps	VCSEL	MMF	100 m	MPO-12	0~70C	Y

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	T_S	-40	-	+85	°C	
Supply Voltage	V_{CC}	-0.5	-	+4.0	V	
Operating Relative Humidity	RH	-	-	+85	%	

Recommend Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Operating Case Temperature	TOP	0		70	degC	
Power Supply Voltage	VCC	3.14	3.3	3.46	V	
Lane Bit Rate			53.125		GBd	With PAM4
Power Consumption	P_D			8	W	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Link Distance with G.652	TD			100	m	

Electrical Characteristics

Parameter	Min	Typical	Max	Unit	Notes
Receiver electrical output characteristics at TP4					
Signaling rate per lane		26.5625		GBd	
AC common-mode output voltage(RMS)		-	17.5	mV	

Differential peak-to-peak output voltage			900	mV	
Near-end SMW(Eye symmetry mask width)		0.265		UI	
Near-end Eye height, differential	70			mV	
Far-end ESMW(Eye symmetry mask width)		0.2		%	
Far-end Eye height, differential	30			mV	
Far-end pre-cursor ISI ratio	-4.5		2.5	%	
Differential output return loss	9.5-0.37f			dB	0.01-8 GHz
	4.75-7.4log 10(f/14)			dB	8-19 GHzGHz
Common to differential mode conversion return loss	22-20(f/25.78)			dB	0.01-12.89 GHz
	15-6log 10(f/25.78)			dB	12.89-19GHz
Differential termination mismatch			10	%	
Transition time(min,20% to 80%)	9.5			ps	
DC common mode voltage	-350		2850	mV	
Transmitter electrical input characteristics at TP1					
Signaling rate per lane		26.5625		GBd	
Differential pk-pk input voltage tolerance	900			mV	
Differential input return loss	9.5-0.37f			dB	0.01-8 GHz
	4.75-7.4lg 10(f/14)			dB	8-19GHz
Differential to common mode input return loss	22-20(f/25.78)			dB	0.01-12.89GHz
	15-6log 10(f/25.78)			dB	12.89-19GHz
Differential termination mismatch			10	%	
Module stressed input test	Per Section 120E.3.4.1 IEEE802.3bs				
Single-ended voltage tolerance range	-0.4		3.3	V	
Common-mode voltage	-350		2850	mV	

Optical Characteristics

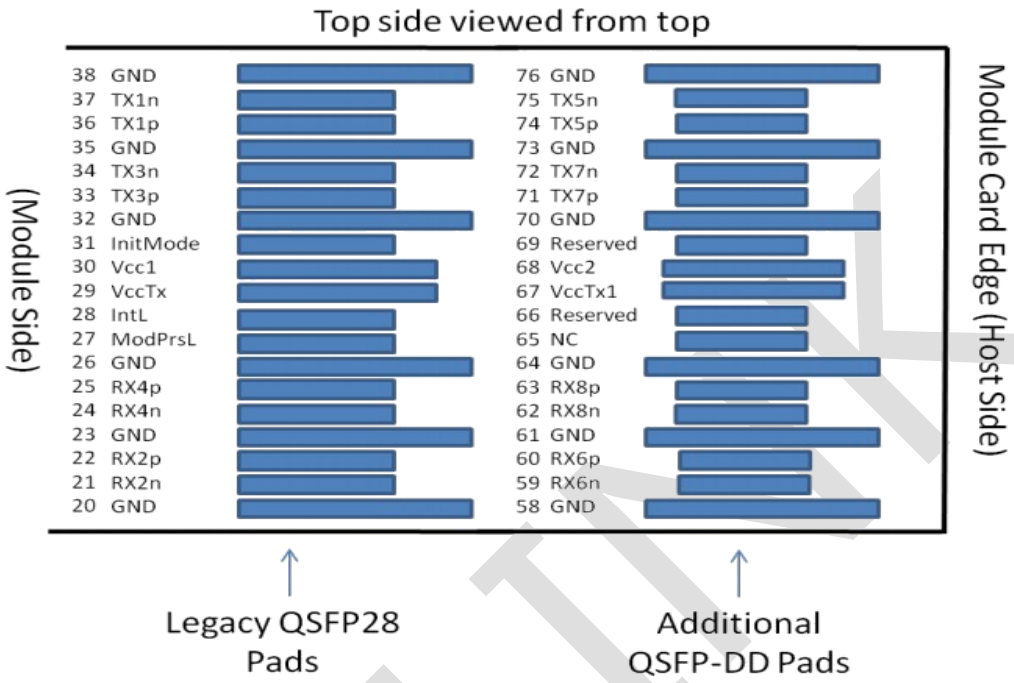
Parameter	Min	Typical	Max	Unit	Notes
Transmitter					

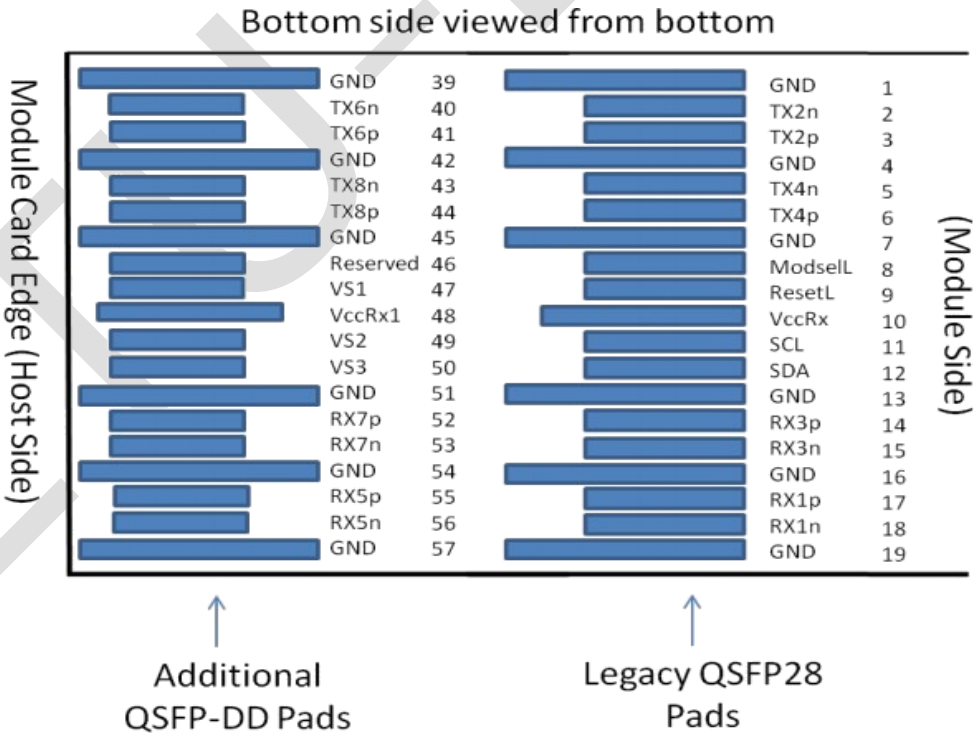
Signaling Rate, each lane (range)	53.125±100ppm			GBd	
Modulation Format	PAM4				
Center Wavelength Range		850		nm	
RMS spectral width			0.6	nm	
Average launch power, each lane	-4.6		4	dBm	
Outer Optical Modulation Amplitude (OMAouter), each lane	-2.6		3.5	dBm	TDECQ<1.8
	TDECQ-4.4		3.5		TDECQ>1.8
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane			4.4	dB	
Extinction ratio, each lane	2.5			dB	
Optical return loss tolerance			12	dB	
Optical Return Loss Tolerance			12	dB	
Average Launch Power per Lane @ TX Off State			-30	dBm	
Relative Intensity Noise12(OMA)			-131	dB/Hz	
Optical Return Loss Tolerance			12	dB	
Receiver					
Signaling Rate, each lane (range)	53.125±100ppm			GBd	
Modulation Format	PAM4				
Center Wavelength Range	840		860	nm	
Damage Threshold	5			dBm	
Average receive power, each lane	-6.4		4	dBm	
Stressed receiver sensitivity (OMAouter), each lane			-2	dBm	
Receive power, each lane (OMAouter)			3.5	dBm	
RX_LOS_Assert	-15.0			dBm	
RX_LOS_De-Assert			-8.9	dBm	
RX_LOS_Hysteresis	0.5			dB	
Receiver sensitivity (OMAouter), each lane	Max(-4.6, SECQ-6.4)			dBm	
Stressed eye closure for PAM4 (SECQ), lane under test		4.4		dB	
SECQ – 10log10(Ceq) (max), lane under test		3.5		dBm	

Digital Diagnostic Monitoring Specifications

Parameter	Unit	Specification
Temperature Monitor absolute error	℃	±3.0
Supply Voltage Monitor absolute error	%	± 5℃
I_bias Monitor absolute error	%	± 10
Received Power (Rx) Monitor absolute error	dB	± 3.0
Transmit Power (Tx) Monitor absolute error	dB	± 3.0

Pin Assignment and Description





PIN	Logic	Symbol	Description	Plug Seq.	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	3B	
7		GND	Ground	1B	1
8	LVTLL-I	ModSelL	Module Select	3B	
9	LVTLL-I	ResetL	Module Reset	3B	
10		VccRx	+ 3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3B	
13		GND	Ground	1B	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/RX_LOS	Interrupt/RX_LOS	3B	
29		VccTx	+3.3 V Power Supply transmitter	2B	2
30		Vcc1	+3.3 V Power Supply	2B	2
31	LVTTL-I	LPMode/Tx_DIS	Low Power Mode/Tx Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	

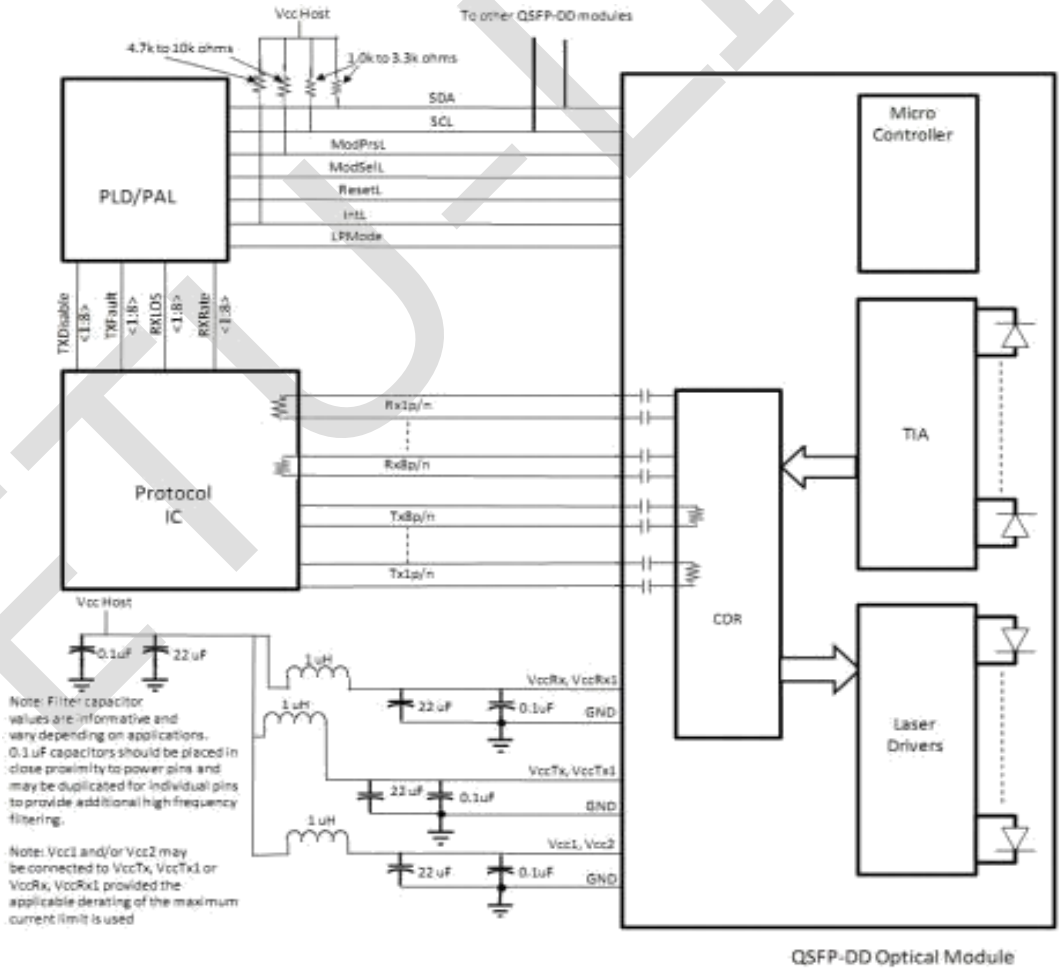
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For future use	3A	3
70		GND	Ground	1A	1

71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

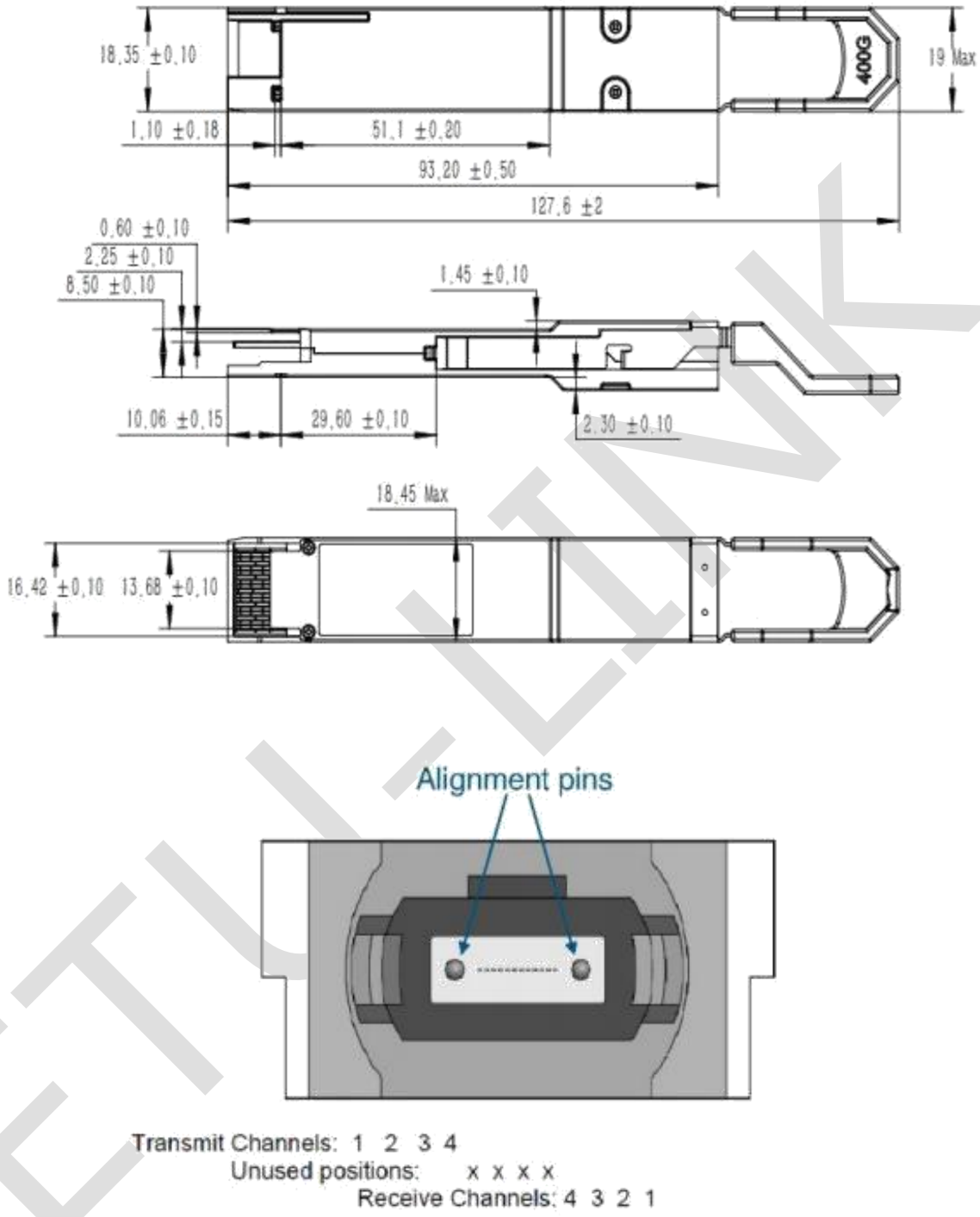
Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6， as per QSFP-DD Hardware Specification V4.0. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pin65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved Pins shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

Recommended Interface Circuit



Mechanical Diagram



Revision History

Version No.	Date	Description
1.0	February 18, 2022	Preliminary datasheet
2.0	September 25,2024	Product upgrades

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