# EQP400-FR4

**400G QSFP112 FR4 Optical Transceiver**

## PRODUCT FEATURES

- **Compliant to QSFP112 MSA V2.0**
- **Compliant with CMIS 5.0**
- **4 CWDM lanes MUX/DEMUX design**
- **100G Lambda MSA 400G-FR4 Specification compliant**
- **4x106. 25Gb/s electrical interface (400GAUI-4)**
- **Up to 2Km transmission over SMF**
- **Maximum power consumption 10W**
- **Duplex LC Receptacle**
- **Single +3.3V power supply**
- **Case temperature range: 0 ~ +70℃**
- **RoHS 2.0 complaint**
-

## APPLICATIONS

- **400G Ethernet**
- **Data Center Interconnect**
- **Enterprise Networking**

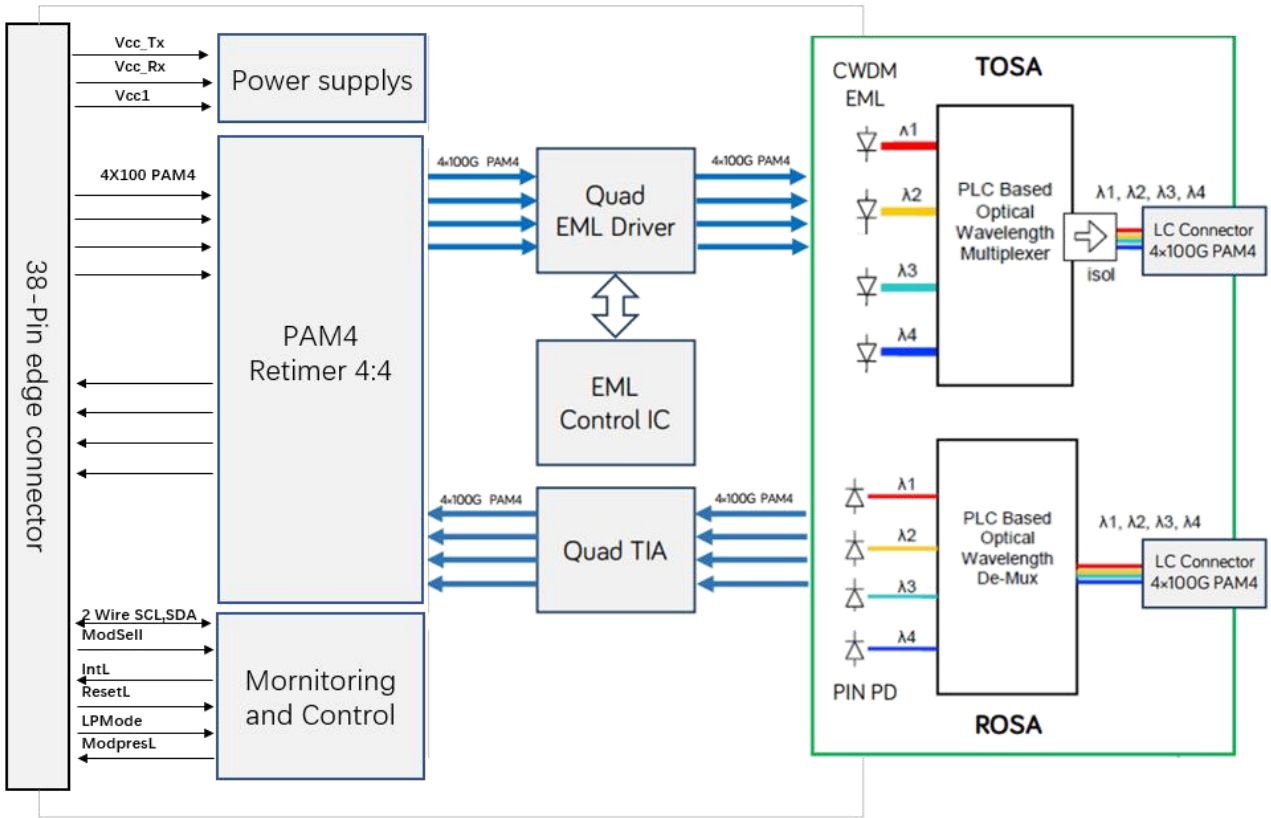
## DESCRIPTIONS

This product is a 400Gb/s QSFP112 optical module designed for 2km optical communication applications. The module converts 4 channels of 100Gb/s (PAM4) electrical input data to 4 channels of CWDM optical signals and multiplexes them into a single channel for 400Gb/s optical transmission.

On the receiver side, the module optically de-multiplexes a 400Gb/s optical input into 4 channels of CWDM optical signals and converts them to 4 channels of 100Gb/s (PAM4) electrical output data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm. Host FEC is required to support up to 2km fiber transmission.

## Module Block Diagram




## Ordering Information

| Part No. | Data Rate(optical) | Laser | Fiber Type | Distance | Optical Interface | Temp | DDMI |
|---|---|---|---|---|---|---|---|
| EQP400-FR4 | 400Gb/s | CWDM EML | SMF | 2KM | LC | 0~70°C | Y |

## Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Storage Temperature Range | TSTG | -40 | +85 | ºC |
| Supply Voltage | VCC | 0 | 4 | V |
| Relative Humidity | RH | 10% to 90% | | |
| | | non-condensing | | |

## Recommended Operating Conditions

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Case Temperature- Operating | TCASE | 0 | 70 | ºC |
| Supply Voltage | Vcc | 3.14 | 3.46 | V |
| Power Consumption | PDISS | | 10 | W |
| Pre-FEC Bit Error Ratio | | | 2.4x10-4 | |
| Link Distance over SMF | | 0.5 | 2000 | M |

## Low Speed Electrical signal

| Parameter | Symbol | Min | Max | Units | Condition |
|---|---|---|---|---|---|
| SCL and SDA | VOL | 0 | 0.4 | V | IOL(max)=3.0mA for fast mode,20mA for Fast-mode plus |
| | VOH | Vcc-0.5 | Vcc+0.3 | V | |
| SCL and SDA | VIL | -0.3 | Vcc*0.3 | V | |
| | VIH | Vcc*0.7 | Vcc +0.5 | V | |
| Capacitance for SCL and SDA I/O pin | Ci | | 14 | pF | |
| Total bus cpacitive load for SCL and SDA | Cb | | 100 | pF | 3.0k Ohms Pull up resistor,max |
| | | | 200 | pF | 1.6k Ohms Pull up resistor,max |
| LPMode/TxDis,Reset and ModeSelL | VIL | -0.3 | 0.8 | V | \|Iin\| </= 125uA for Vin < Vcc |
| | VIH | 2 | Vcc + 0.3 | V | |
| IntL/RxLOS | VOL | 0 | 0.4 | V | IOL=2.0mA |
| | VOH | VCC - 0.5 | VCC + 0.3 | V | 10k ohms pull-up to Host Vcc |
| ModPrsL | VOL | 0 | 0.4 | % | IOL=2.0mA |
| | VOH | | | dB | ModPrsL can be implemented as a short-circuit to GND on the module |

## High Speed Electrical signal

| Parameter | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|
| Receiver electrical output characteristics at TP4 | | | | | |
| Signaling rate per lane | | 53.125 | | GBd | |
| AC common-mode output voltage(RMS) | | - | 17.5 | mV | |
| Differential peak-to-peak output voltage | | | 900 | mV | |
| Near-end ESMW (Eye symmetry mask width) | | TBD | | UI | |
| Near-end Eye height, differential | 24 | | | mV | |
| Near-end vertical eye closure | | | 7.5 | dB | |
| Far-end ESMW (Eye symmetry mask width) | | TBD | | UI | |
| Far-end Eye height, differential | 24 | | | mV | |
| Far-end vertical eye closure | | | 7.5 | dB | |
| Far-end pre-cursor ISI ratio | | TBD | | % | |
| Common mode to differential conversion return loss | 802.3ck 120G-1 | | | dB | |
| Effective return loss | TBD | | | dB | |
| Differential termination mismatch | | | 10 | % | |
| Transition time (min, 20% to 80%) | | TBD | | ps | |
| DC common mode voltage | -350 | | 2850 | mV | |
| Transmitter electrical input characteristics at TP1 | | | | | |
| Signaling rate, per lane | | 53.125 | | GBd | |
| Differential pk-pk input voltage tolerance | 900 | | | mV | |
| Common-mode to differential return loss | 802.3ck Equation(120G-1) | | | | |
| Effective return loss | TBD | | | | |
| Differential termination mismatch | | | 10 | % | |
| Module stressed input test | See 120G.3.4.1 | | | | |
| Single-ended voltage tolerance range | -0.4 | | 3.3 | V | |
| DC common-mode voltage | -350 | | 2850 | mV | |

## Optical and Characteristics

| Transmitter Parameter | Lane | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| **Transmitter** | | | | | |

| | | | | | |
|---|---|---|---|---|---|
| Lane Wavelength Range | Lane 0 | 1264.5 | 1271 | 1277.5 | nm |
| | Lane 1 | 1284.5 | 1291 | 1297.5 | nm |
| | Lane 2 | 1304.5 | 1311 | 1317.5 | nm |
| | Lane 3 | 1324.5 | 1331 | 1337.5 | nm |
| Average launch Power per lane | | -3.2 | | 4.4 | dBm |
| Total Average launch power | | | | 10.4 | dBm |
| Outer Optical Modulation Amplitude (OMAouter), each lane<br>for TDECQ <1.4 dB<br>for 1.4 dB ≤TDECQ ≤3.4 dB | | -0.2<br>–1.6 + TDECQ | | 3.7 | dBm |
| Difference in launch power between any two lanes (OMAouter) | | | | 3.9 | dB |
| Average Launch Power per Lane @ TX Off State | | | | -16 | dBm |
| Transmitter and Dispersion Eye Closure for PAM4, each Lane | | | | 3.4 | dB |
| Extinction Ratio | | 3.5 | | | dB |
| Relative Intensity Noise (OMA) | | | | -136 | dB/Hz |
| Side-Mode Suppression Ration (SMSR) | | 30 | | | dB |
| Optical Return Loss Tolerance | | | | 17.1 | dB |
| Transmitter Reflectance | | | | -26 | dB |
| Transmitter Output Power Monitoring Accuracy | | -3 | | 3 | dB |
| Transmitter transition time | | | | 17 | ps |
| **Receiver** | | | | | |
| Lane Wavelength Range | Lane 0 | 1264.5 | 1271 | 1277.5 | nm |
| | Lane 1 | 1284.5 | 1291 | 1297.5 | nm |
| | Lane 2 | 1304.5 | 1311 | 1317.5 | nm |
| | Lane 3 | 1324.5 | 1331 | 1337.5 | nm |
| Damage Threshold | | 5.4 | | | dBm |
| Average Receive Power, each lane | | -7.2 | | 4.4 | dBm |
| Receiver Power, each lane (OMA) | | | | 3.7 | dBm |
| Receiver Reflectance | | | | -26.0 | dB |
| Difference in receive Power between any Two Lanes(OMAouter) | | | | 4.1 | dBm |
| Receiver Sensitivity each lane (OMAouter) | | | | max(-4.6,SECQ-6.0) | dBm |
| Stressed Receiver Sensitivity (OMAouter), each | | | | -2.6 | dBm |
| RX_LOS_Assert Min/Max | | -20.0 | | | dBm |

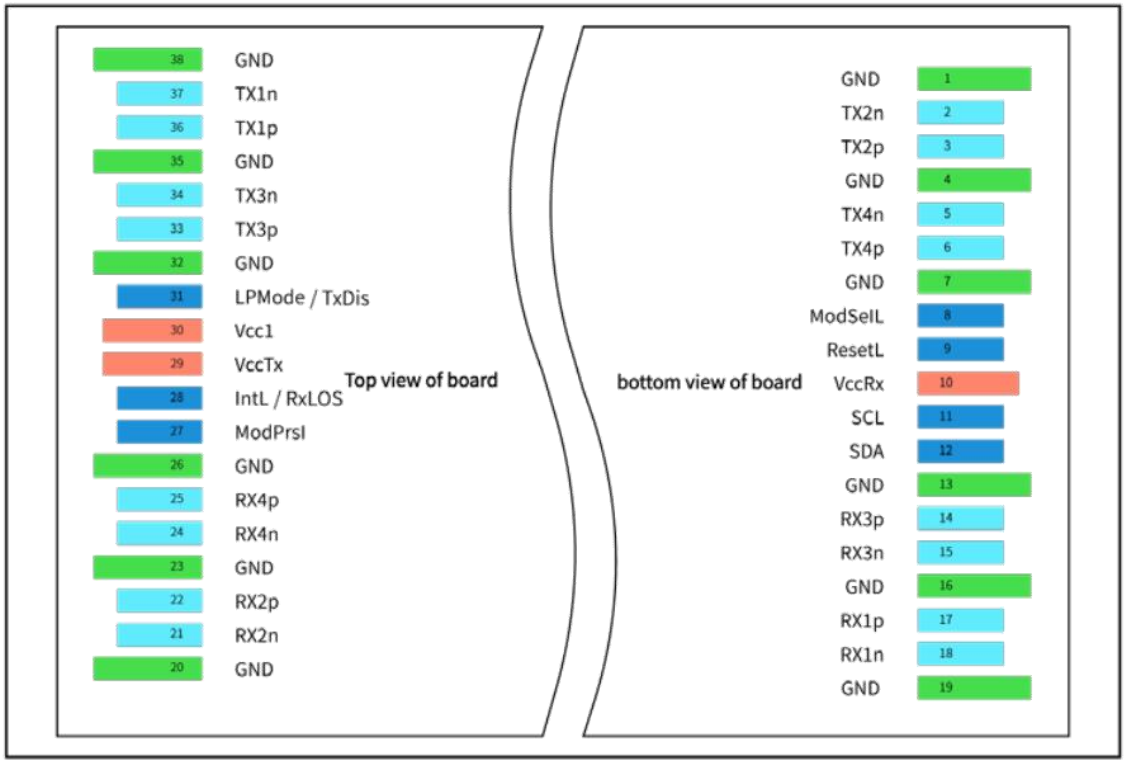
| | | | | | |
|---|---|---|---|---|---|
| RX_LOS_De-Assert Min/Max | | | | -10.3 | dBm |
| RX_LOS_Hysteresis | | 0.5 | | | dB |

## Digital Diagnostics

| Parameters | Unit | Specification |
|---|---|---|
| Temperature Monitor absolute error | °C | ± 3 |
| Supply Voltage Monitor absolute error | % | ± 5 |
| I_bias Monitor absolute error | % | ± 10 |
| Received Power (Rx) Monitor absolute error | dB | ± 3.0 |
| Transmit Power (Tx) Monitor absolute error | dB | ± 3.0 |

## Pin Diagram

QSFP112 Edge Connector and Pinout Description




## Pin Definitions

| Pin No. | Logic | Symbol | Description | Plug Sequence | Notes |
|---|---|---|---|---|---|
| 1 | | GND | Ground | 1 | 1 |
| 2 | CML-I | TX2n | Transmitted Inverted Data Input | 3 | |

| | | | | | |
|---|---|---|---|---|---|
| 3 | CML-I | TX2p | Transmitted Non-Inverted Data Input | 3 | |
| 4 | | GND | Ground | 1 | 1 |
| 5 | CML-I | TX4n | Transmitted Inverted Data Input | 3 | |
| 6 | CML-I | TX4p | Transmitted Non-Inverted Data Input | 3 | |
| 7 | | GND | Ground | 1 | 1 |
| 8 | LVTTL-I | ModSeil | Module Select | 3 | |
| 9 | LVTTL-I | ResetL | Module Reset | 3 | |
| 10 | | Vcc Rx | +3.3 VDC Receiver Power Supply | 2 | 2 |
| 11 | LVCMOS-I/O | SCL | Serial Clock for I2C Interface | 3 | |
| 12 | LVCMOS-I/O | SDA | Serial Data for I2C Interface | 3 | |
| 13 | | GND | Ground | 1 | 1 |
| 14 | CML-O | RX3p | Receiver Non-Inverted Data Output | 3 | |
| 15 | CML-O | RX3n | Receiver Inverted Data Output | 3 | |
| 16 | | GND | Ground | 1 | 1 |
| 17 | CML-O | RX1p | Receiver Non-Inverted Data Output | 3 | |
| 18 | CML-O | RX1n | Receiver Inverted Data Output | 3 | |
| 19 | | GND | Ground | 1 | 1 |
| 20 | | GND | Ground | 1 | 1 |
| 21 | CML-O | RX2n | Receiver Inverted Data Output | 3 | |
| 22 | CML-O | RX2p | Receiver Non-Inverted Data Output | 3 | |
| 23 | | GND | Ground | 1 | 1 |
| 24 | CML-O | RX4n | Receiver Inverted Data Output | 3 | |
| 25 | CML-O | RX4p | Receiver Non-Inverted Data Output | 3 | |
| 26 | | GND | Ground | 1 | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present | 3 | |
| 28 | LVTTL-O | IntL/RxLOS | Interrupt/optional RxLOS | 3 | |
| 29 | | Vcc Tx | +3.3 VDC Transmitter Power Supply | 2 | 2 |
| 30 | | Vcc1 | +3.3 VDC Power Supply | 2 | 2 |
| 31 | LVTTL-I | LPMode/Tx dis | Low Power Mode/optioanl Tx Disable | 3 | |
| 32 | | GND | Ground | 1 | 1 |
| 33 | CML-I | TX3p | Transmitted Non-Inverted Data Input | 3 | |
| 34 | CML-I | TX3n | Transmitted Inverted Data Input | 3 | |
| 35 | | GND | Ground | 1 | 1 |
| 36 | CML-I | TX1p | Transmitted Non-Inverted Data Input | 3 | |
| 37 | CML-I | TX1n | Transmitted Inverted Data Input | 3 | |
| 38 | | GND | Ground | 1 | 1 |

Note :

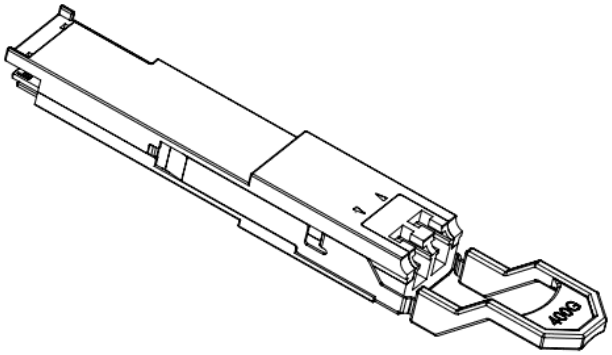
1: GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all volt ages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

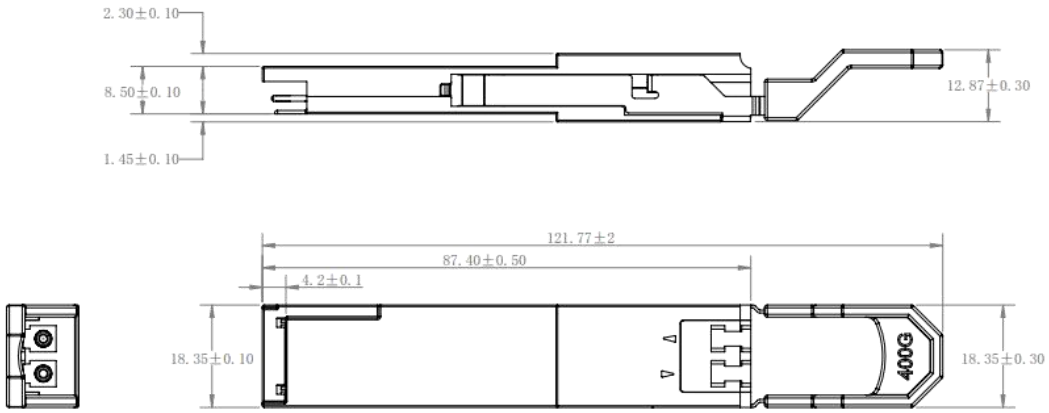
2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements, defined for the host side of the Host Edge Card Connector, are listed in Table 4. Recommended host board power supply filtering is shown in Figure 4. Vcc Rx, Vcc1and Vcc Tx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).

## Mechanical Diagram

Mechanical Drawings

Pull Tab Color:Blue
Pantone:300U




## Revision History

| Version No. | Date | Description |
|---|---|---|
| 1.0 | Aug 20, 2024 | Preliminary datasheet |